PATENT APPLICATION
DOCKET NO.: 200207724-1

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the pending claims.

1. (Currently Amended) A system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement, said clock synchronizer arrangement for effectuating data transfer between a core clock domain and a bus clock domain wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio, comprising:

means disposed in a bus clock synchronizer controller portion for generating a set of inter-controller clock relationship control signals, said means in said bus clock synchronizer controller portion being operable responsive to a SYNC pulse that is sampled in said bus clock domain by said bus clock signal; and

means disposed in a core clock synchronizer controller portion operating responsive to said set of inter-controller clock relationship control signals for synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal, wherein said means in said core clock

synchronizer controller portion is operable responsive to said SYNC pulse that is sampled in said core clock domain by said core clock signal.

Claim 2. (Canceled)

3. (Currently Amended) The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim [[2]] 1, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said core clock signal is at least substantially coincident with a rising edge in said bus clock signal.

Claim 4. (Canceled)

5. (Currently Amended) The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim [[4]] 1, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of an initial sequence and cycle with respect to said bus clock signal.

6. (Original) The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 5, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of a clock frequency ratio associated with said bus clock and core clock signals.

7. (Original) The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 6, wherein said set of inter-controller clock relationship control signals includes a control signal that is derived by delaying said sampled SYNC pulse by a number of bus clock cycles.

8. (Original) The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 7, wherein said means disposed in said core clock synchronizer controller portion includes a sync_ratio sampling means for sampling said control signal indicative of a clock frequency ratio associated with said bus clock and core clock signals.

9. (Original) The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 7, wherein said means disposed in said core clock synchronizer controller portion includes a sequence sampling means for sampling said control signal indicative of an initial sequence and cycle with respect to said bus clock signal.

10. (Original) The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 7, wherein said means disposed in said core clock synchronizer controller portion includes a delayed_sync sampling means for sampling said control signal that is derived by delaying said sampled SYNC pulse by a number of bus clock cycles.

11. (Original) The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 7, further including means disposed in said core clock synchronizer controller portion for determining that said clock frequency ratio is stable.

12. (Currently Amended) A method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement, said clock synchronizer arrangement for effectuating data transfer between a core clock domain and a bus clock domain wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio, comprising:

generating a set of inter-controller clock relationship control signals in a bus clock synchronizer controller portion operable responsive to a SYNC pulse that is sampled in said bus clock domain by said bus clock signal; and

responsive to said inter-controller clock relationship control signals, synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal in a core clock synchronizer controller portion operable responsive to said SYNC pulse that is sampled in said core clock domain by said core clock signal.

Claim 13. (Canceled)

14. (Currently Amended) The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim [[13]] 12, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said core clock signal is at least substantially coincident with a rising edge in said bus clock signal.

Claim 15. (Canceled)

16. (Currently Amended) The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim [[15]] 12, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of an initial sequence and cycle with respect to said bus clock signal.

17. (Original) The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 16, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of a clock frequency ratio associated with said bus clock and core clock signals.

18. (Original) The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 17, wherein said set of inter-controller clock relationship control signals includes a control signal that is derived by delaying said sampled SYNC pulse by a number of bus clock cycles.

19. (Original) The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 18, wherein said operation of synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal includes sampling said control signal indicative of a clock frequency ratio associated with said bus clock and core clock signals.

20. (Original) The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 18, wherein said operation of synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal includes sampling said control signal indicative of an initial sequence and cycle with respect to said bus clock signal.

21. (Original) The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 18, wherein said operation of synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal includes sampling said control signal that is derived by delaying said sampled SYNC pulse by a number of bus clock cycles.

22. (Original) The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 18, further including determining that said clock frequency ratio is stable for synchronizing cycle and sequence information associated with said core clock signal.

Claims 23 - 31. (Canceled)